**Internal Assessment Question Paper – 3**

**M.S. Ramaiah Institute of Technology**

**(Autonomous Institute, Affiliated to VTU)**

**Department of CSE**

**Programme :** B.E **Term:** Jan- May 2016 **Date:** 5-5-2016

**Course:** Computer Organization **Course Code:** CS1541  **CIE:** Test 3

**Sem:** IV **Sec:** A, B & C **Max Marks:** 30 **Time:** 9:30–10:30 am

**Portions for Test:** (L35-L52)

**Instructions to Candidates:** Mobiles, smart watches or any electronic gadgets are strictly banned.

Answer two questions, 1st Question is compulsory.

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| **Sl#** | **Question** | **Marks** | **Bloom’s Level** | **CO Mapping** |
| **1** | 1. Differentiate between write-through and write-back cache techniques. | 5 | Analyze | CO4 |
| 1. Assume a cache consists of 8 one word blocks. Find the number of misses for the following sequence of block addresses 0,8,0,6,7,2,1,6 & 8 using the following cache mapping techniques   i) Direct- mapped ii)Two-way set-associative iii)Fully associative cache | 5 | Apply | CO4 |
| 1. Describe dependability, availability and reliability measures for I/O systems. | 5 | Understand | CO5 |
| **2** | 1. Describe how cache handles data and instruction misses. | 5 | Understand | CO4 |
| 1. With a neat diagram explain the address translation using TLB in virtual memory implementation. | 5 | Understand | CO4 |
| 1. Compute an average time to read or write a 1024-byte sector for a typical disk rotating at 7200 RPM? The advertised average seek time is 11 ms, the transfer rate is 34 MB/sec, and the controller overhead is 480MBits/sec. Assume that the disk is idle so that there is no waiting time. | 5 | Apply | CO5 |
|  | **OR** |  |  |  |
| **3** | 1. Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate at 4GHz. Assume a main memory access time of 200ns, including all the miss handling.   Suppose a miss rate per instruction at the primary cache is 4%. Calculate how much faster will the processor be if we add a secondary cache that has a 5ns access time for hit or miss and can reduce miss rate to main memory to 0.8% | 5 | Apply | CO4 |
| 1. Describe with a neat diagram how system handles the page faults in virtual memory implementation. | 5 | Understand | CO4 |
| 1. List out the steps that must taken by the operating system to handle the interrupt. | 5 | Remember | CO5 |

**Course Outcomes meant to be assessed by the IA Test-III**:

CO4: Assess the cache memory performance and also recognize the advantages of using virtual memory technique.

CO5: Demonstrate Interfacing of I/O devices with processor memory and operating system including data transfer between memory and I/ devices.